Development of Graphene for High Frequency Electronics

J. A. Robinson, D. Snyder, Mark Fanton, M. J. Hollander, M. Labella, Z. Hughes, K. Trumbull, R. Cavalero, B. Weiland, E. Hwang, and S. Datta

The Pennsylvania State University, University Park, PA, U.S.A
jrobinson@psu.edu

Graphene's high carrier mobility[1], large saturation current[2], low noise, and superior scalability make it of interest as a channel material for RF-FET applications. The practicality and success of such a technology depends on the ability to, first, regularly and controllably synthesize graphene, second, integrate it with metals and dielectrics in a reproducible manner, and, finally, to develop device designs that take advantage of (or overcome) graphene's unique properties while minimizing performance-limiting parasitics. In this talk, we will provide insight into ultra-large area growth, integration of graphene with ultra-thin dielectrics (EOT ~ 1nm), and how growth and device processing effect the transport properties of epitaxial graphene.

Graphene synthesis is accomplished on SiC (Figure 1) and Sapphire up to 100mm wafers, with excellent uniformity (Figure 2). Graphitization of SiC(0001) is achieved by low-pressure sublimation of Si from the Si-face of semi-insulating 6H-SiC (II-VI, Inc.) at 1600°C and mediated by an Ar atmosphere.[3] Graphene films grown under these conditions are primarily one- to two-layers thick according to Raman spectroscopy and transmission electron microscopy,[4] with a D/G peak ratio of 0.07 ± 0.03. Direct growth of graphene on sapphire is accomplished via the decomposition of methane at 1425 - 1600°C, where film nucleation and quality are found to be a strong function of methane concentration, growth time, and growth temperature.[5] Raman spectroscopy confirms, for the first time, the formation of monolayer and bilayer graphene on sapphire, with improved structural quality as deposition temperature increases.

In addition to synthesis of large area, high quality graphene, the successful implementation of a graphene-based electronic technology must address low resistance metal/graphene contacts, and the integration of graphene with high-k dielectrics. We have developed a robust method for forming high quality ohmic contacts to graphene, which improves the contact resistance by nearly 6000x compared to untreated metal/graphene interfaces.[6] Optimal specific contact resistance for treated Ti/Au contacts is found to average $5x10^{-8}$ Ohm-cm^2, demonstrating a significant improvement in ultimate resistance compared to current technology. It is found that most metallizations result in similar contact resistances in this work (Figure 3), regardless of the work function difference between graphene and the metal over layer, which is explained by the chemical and structural modification of graphene during device processing.

Finally, we discuss the successful integration of ultra-thin high-k dielectrics and their impact on graphene transport. All oxides deposited via atomic layer deposition require some type of seeding method. Additionally, heterostructures (seed ≠ overlayer) have deleterious effects on Hall mobility while homostructures can lead to an increase in Hall mobility (Figure 4). Doping appears to be material dependent and varies with film thickness. Importantly, 5nm thick EBPVD HfO_2 gate dielectrics with an EOT of ~1nm are successfully demonstrated and show improved Hall mobility, on-off ratio, and transconductance relative to Al_2O_3 gates and heterostructure gates comprised of various dielectrics (Figure 5).

References

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Figures

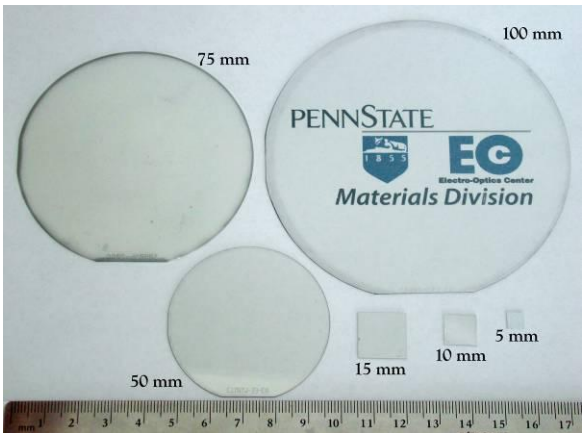

Figure 1: Photographic image of graphene grown SiC(0001) wafers up to 100 mm

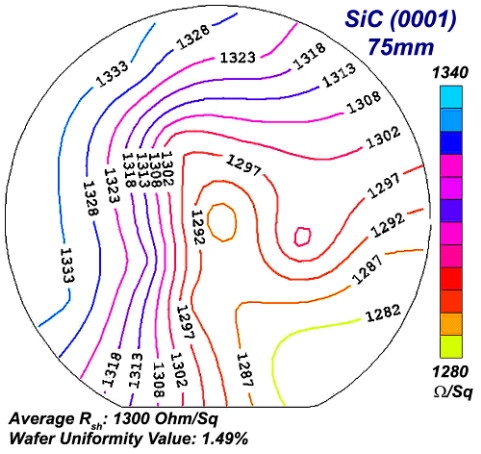

Figure 2: Sheet resistance (Ohm/sq) map of a 75mm graphene wafer illustrating high uniformity

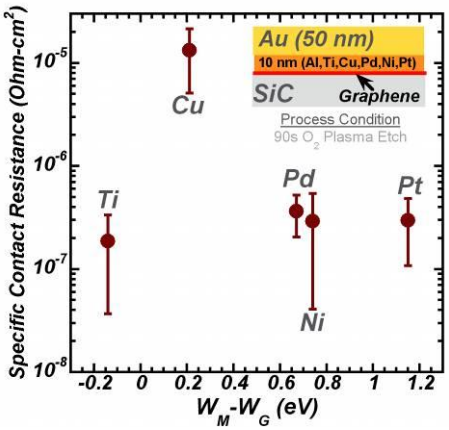

Figure 3: Specific contact resistance of various metals versus graphene/metal work function difference.

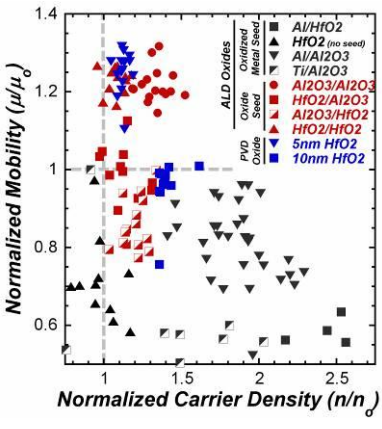

Figure 4: Normalized Graphene carrier mobility vs. density as a function of dielectric overlayer.

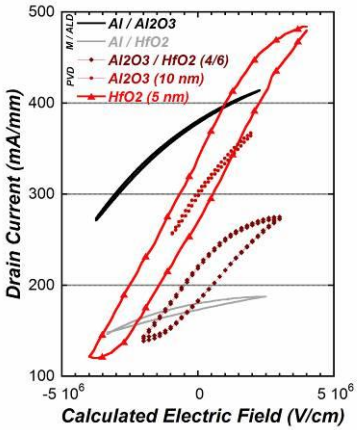

Figure 5: Graphene transistor drain current vs. gate electric field. 5 nm HfO_2 exhibits superior transport characteristics compared to all other dielectrics.